ABSTRACT

A scheme for reducing jitter in high-speed digital communication by adaptively controlling the loop bandwidth of a receiver PLL to reduce the relative jitter between the recovered data and clock. The scheme uses phase pointer activity to represent the relative jitter. The phase pointer activity is measured and used to control the receiver PLL loop bandwidth. The receiver PLL loop bandwidth is repeatedly incremented or decremented by a step size based on the comparison between a newly measured activity value and the old activity value, until the phase pointer activity reaches a minimum. Because the PLL performance requirement of the transmitter can be relaxed, compatibility with legacy transmitters and multi-vendor transmitters is enhanced. Because tight control of fabrication process parameters of PLLs may be relaxed, the fabrication yield may also be improved.